REMARKS

This responds to the Office Action mailed on February 17, 2006.

Claims 1 – 4, 7, 9, 15 – 18 and 20 – 22 are amended, no claims are canceled, and claims 24 – 27 are added; as a result, claims 1 – 13 and 15 - 27 are now pending in this application.

§103 Rejection of the Claims

Claims 1 - 4, 6-13 and 15 - 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wiser et al. (U.S. 6,385,596) in view of Hardjono (U.S. 6,182,214), further in view of Johnston (U.S. 6,373,946), further in view of Arnold (U.S. 6,175,924), and further in view of Nakagawa (U.S. 2002/0016775). Claim 5 was also rejected under 35 U.S.C. § 103(a) as being unpatentable over Wiser et al., Hardjono, Johnston, Arnold and Nakagawa, and further in view of Howard et al. (U.S. 2002/0069365).

Applicant's claims, as amended, are directed to a method, a multiprocessor system or a wireless communication device with two or more processors that include a security processor and a communication processor located within a processor area of an integrated circuit. The rejections of all of Applicant's pending claims rely on Arnold for teaching two processors. Applicants respectfully disagree with this interpretation of Arnold as applied to Applicant's claims and submit that Arnold disclosures only a computer system with a single microprocessor #15, and a *single* processor #51 within a *separate* security module #13 (see Arnold FIG. 1). Although Arnold's system has two processors, **there is no teaching, suggestion, or motivation in Arnold to provide a single device or system with two or more processors within a single processor area of an integrated circuit**. Arnold's processors communicate over bus 17, which is a standard computer system bus. This allows signals communicated over bus 17 to be easily intercepted. This is a serious drawback when the information on the bus is decrypted content that should not be copied.

Applicant's independent claims 1, 16, 21 and 25, on the other hand, recite that a security processor and a communication processor are located within a processor area of

an integrated circuit. Applicant's claims 1, 16, 24 and 25 further recite that communications between the security processor and the communication processor take place within the processor area to inhibit unauthorized interception of the decrypted content and interception of the key-share stored in the processor area. Limiting certain communication to within the processor area of an integrated circuit ***significantly inhibits the possibility of interception*** of decrypted information that is generated by the security processor. Providing the security processor and the communication processor at separate remote locations (as taught by Arnold) ***teaches away*** from this advantage of Applicant's claimed invention by allowing the decrypted content to be vulnerable to interception and illegal copying. In view of this, Applicant submits that Arnold teaches away from Applicant's claims.

Claim 20 (as previously presented) recites that the security processor, the application processor, and the communication processor are part of a processor area and fabricated on an application specific integrated circuit (ASIC). Independent claims 1, 16 have been amended to recite that the security processor and the communication processor are located within a processor area of an integrated circuit. Claim 9 has been amended to recite that the security processor and the communication processor are fabricated as an application specific integrated circuit (ASIC). Claim 21 recites a processor area of an integrated circuit having a communications processor and security processor.

In view of the above, Applicant submits that the combination of Wiser et al., Hardjono, Johnston, Arnold, Nakagawa, and Howard does not result in Applicant's claimed invention. In further view of the above, Applicant's that Arnold teaches away from Applicant's claimed invention eliminating any motivation for the combination. In view of these remarks and the amendment to the claims, Applicants believe that the rejection of claims 1 – 13 and 15 – 23 has been overcome, and that claims 1 – 13, and 15 – 27 are in condition for allowance.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, Greg Gorrie at (480) 659-3314, or Applicant's below-named representative to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 17 day of April 2006.

Chris Hammond
Name

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